REMARKS/ARGUMENT

In the present application claims 1-19 were examined. Claims 1-19 stand rejected. Claims 1-19 are pending in the present application. No new matter is added.

Claim Rejections - 35 U.S.C. §103

The Office Action states that claims 16-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Miyasaka (U.S. Patent No. 6,124,154) in view of Kuo et al. (U.S. Patent No. 5,981,347). In particular, the Office Action states that Miyasaka discloses all the elements of claims 16-19 with the exception of the specific processing conditions of a polysilicon layer and a thermal oxidation and densification process, and performing a first anneal procedure subsequent to growing the first dielectric layer of a TFT. The Office Action further states that Kuo et al. supply the missing elements in an obvious combination to one of ordinary skill in the art. Applicants respectfully traverse the rejection.

In the present application, Applicants have repeatedly argued that none of the cited prior art references disclose the use of a rough polysilicon layer as an active layer in a thin film transistor device. This element is clearly recited in claims 16-19:

> providing an insulating substrate; and
>
> forming a rough polysilicon layer on said insulating substrate.

The Office Action states that Miyasaka discloses the use of a polysilicon layer, citing col. 17, lines 42-45 of the disclosure by Miyasaka. However, a review of that portion of the disclosure by Miyasaka fails to produce any usable information regarding the use of polysilicon. Miyasaka states in col. 17, lines 42-45:

> next, in the fourth process step ST4A, the substrate on which the polyscrystalline semiconductor layer and the first gate insulator layer have been formed is hydrogenated (ST41).

A polycrystalline semiconductor layer is distinctly different from a polysilicon layer, especially because of the difference in smoothness in the two different types of layer. Applicants have repeatedly stated that polysilicon semiconductor layers are much rougher, and especially in the present invention, than are any other types of semiconductor layers recited in the prior art, including polycrystalline silicon layers, single crystalline layers, amorphous silicon and combinations of amorphous and polycrystalline silicon layers. It is the particular nature of the roughness of polysilicon layers in a TFT that the present invention seeks to overcome by providing a specific and novel process for depositing a gate dielectric layer that overcomes the drawbacks of the prior art.

The Office Action states that the disclosure by Kuo et al. discloses performing a high temperature anneal after gate oxide formation to activate the source/drain regions, but this disclosure is, in fairness, neither pertinent to the present invention recited in claims 16-19, nor obvious to combine with the disclosure by Miyasaka to produce the invention recited in claims 16-19. The disclosure by Kuo et al. provides for annealing an implanted semiconductor substrate in the presence of a gate dielectric layer that was used to mask the substrate implantation. Accordingly, Kuo et al. does not teach any type of processing conditions with respect to a polysilicon layer, thermal oxidation densification process, or the application of such techniques to a TFT. Therefor, the combination of the disclosures by Miyasaka and Kuo et al. do not produce all of the elements recited in claims 16-19, and do not teach one of ordinary skill in the art how to arrive at the recited invention. Indeed, owing to the lack of any discussion whatsoever regarding the use of a polysilicon layer, the present invention recited in claim 16 cannot be said to be at all obvious over the disclosures by Miyasaka and Kuo et al., either alone or in combination.

In addition, as noted above, it would not have been obvious to one of ordinary skill in the art to combine the disclosures by Miyasaka and Kuo et al. to achieve the present invention. Kuo et al. is directed to forming a hot carrier effect MOSFET, and is drawn from a totally different field of art than is the present invention for forming thin film transistors. Accordingly, one of ordinary skill in the art would not look to the disclosure by Kuo et al. to supplement the disclosure by Miyasaka to arrive at the present invention recited in claims 16-19, especially since

the disclosures by Miyasaka and Kuo et al. do not suggest such combination between the two. Accordingly, the requirements for a *prima facie* case of obviousness have not been met based on the disclosures by Miyasaka and Kuo et al. with regard to claims 16-19. MPEP 2142 et seq. Indeed, even if the disclosures by Miyasaka and Kuo et al. could be combined, the result would either not be a thin film transistor, or would be a thin film transistor with an enhanced hot carrier effect, which does not describe the present invention recited in claims 16-19. Accordingly, the rejection of claims 16-19 under 35 U.S.C. §103(a) over the disclosures by Miyasaka and Kuo et al. is believed to be overcome, and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Applicants note that the Office Action also states that the disclosure by Yamazaki (U.S. Patent No. 6,306,213) discloses ranges that would have been obvious for one of ordinary skill in the art to apply in order to obtain the present invention. However, the disclosure by Yamazaki is apparently not applied in the rejection of claims 16-19, but cited for the premise that a gate dielectric layer with a thickness of between 500-2000Å is known. Again, Applicants note that Yamazaki failed to disclose the use of a gate dielectric layer over a polysilicon layer, but rather discusses a crystallized semiconductor layer that is obtained prior to deposition of a gate dielectric layer (col. 7, line 17-col. 8, line 17). Accordingly, Applicants submit that the disclosure by Yamazaki should not be considered to teach one of ordinary skill in the art the use of an obvious range in a process in which the parameters and materials are entirely different. To the extent that the Office Action seeks to combine the disclosure by Yamazaki with any other cited prior art, Applicants note that the disclosure by Yamazaki has not been used to reject any of the claims in the present application, and further note that it would neither be obvious in view of Yamazaki to arrive at the present invention recited in the claims of the present application, nor to combine Yamazaki with any of the other cited prior art in the application to anticipate or make obvious the present invention recited in the claims of the present application.

Claims 1-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,037,199) in view of Doklan et al. (U.S. Patent No. 4,851,370) or in view of Kuo et al. The Office Action states that Huang et al. disclose all of the elements recited in claims 1-19, with the exception of a composite gate dielectric layer with a first thermally grown

oxide layer, followed by an annealing process, a second thermally deposited oxide layer using a TEOS source, and second subsequent anneal, which disclosure is supplied by either Doklan et al. or Kuo et al., in an obvious combination for one of ordinary skill in the art. Applicants respectfully traverse the rejection.

The Office Action states that Huang et al. shows a semiconductor layer of polysilicon on an insulating substrate, overlaid with a gate dielectric layer. However, a review of the disclosure by Huang et al. reveals that the description is directed to a method for fabricating DRAM devices, rather than forming TFT devices, which is stated in at least the preamble of claim 1. DRAM devices are distinctly different from TFT devices. Indeed, Huang et al. disclose a DRAM with an insulating substrate on top of a semiconductor substrate, over which an active device is constructed. Accordingly, Huang et al. does not show the formation of a composite gate dielectric layer for a thin film transistor.

Furthermore, the Office Action states that Huang et al. disclose a semiconductor polysilicon layer overlaid with a gate dielectric layer. However, the description by Huang et al. provides absolutely no disclosure whatsoever for such a structure. Although Huang et al. appear to disclose a polysilicon layer at an initial stage of a process, the polysilicon layer is converted to a single crystalline layer prior to the deposition of any other layer over the single crystalline layer. In addition, further layers over the single crystalline layer are used as masks to permit the removal of any polysilicon or amorphous silicon remaining in the DRAM cell. That is, a gate dielectric layer is never grown over a polysilicon layer in the structure provided by Huang et al. (col. 3, lines 29-53, and Fig. 4). However, this structure is clearly recited in claim 1 of the present invention.

Similarly, the disclosure by Doklan et al. fails to teach or suggest the use of a polysilicon layer that is overlaid by a gate dielectric layer. Accordingly, the disclosure by Doklan et al. cannot in fairness be said to teach or suggest the elements of claims 1-19, which include:

> providing an insulating substrate;

providing a rough polysilicon layer on said insulating substrate; and

thermally growing a first gate dielectric layer, in a furnace, on said polysilicon layer.

Accordingly, the disclosure by Huang et al. lacks elements recited in at least claim 1 of the present invention.

The Office Action further states that Huang et al. lacks anticipation of forming a composite gate dielectric layer comprising a first thermally grown oxide layer, followed by an annealing process, a second thermally deposited oxide layer using a TEOS source and a second subsequent anneal. The Office Action states that Doklan et al. provides a disclosure that, in combination with the disclosure by Huang et al., provides the invention recited in claims 1-19. However, this conclusion is unsupported by the content of the disclosures by Huang et al. and Doklan et al. As stated above, Huang et al. fails to disclose a gate dielectric layer disposed over a rough polysilicon layer. Accordingly, even with the combination of Doklan et al., the cited prior art references still fail to teach a number of the elements recited in at least claim 1. Indeed, the disclosure by Doklan et al. is silent with regard to the nature of any semiconductor layer underlying a gate dielectric layer, and therefore cannot teach the elements of the present invention recited in claims 1-19. Similarly, and as discussed above, Kuo et al. fail to disclose a formation of a gate dielectric layer on a polysilicon layer in a TFT device.

The Office Action further states that it would have been obvious to combine the disclosures by Huang et al. and Doklan et al., or Kuo et al. to arrive at the present invention recited in claims 1-19. However, as noted above, the disclosure by Huang et al. is directed to a creation of DRAM cells that do not suffer from a gate dielectric breakdown problem. Accordingly, it would not have been obvious to obtain the disclosure by Doklan et al. to combine the same with that of Huang et al. to arrive at the present invention, which recites the formation of a gate dielectric layer for a TFT device. Because TFT devices and DRAM cells are in distinctly different fields of art, Applicant respectfully submits that one of ordinary skill in the art

would not be motivated, or receive any suggestion based on the disclosure by Huang et al., to apply the teachings of Doklan et al. to a DRAM cell device to arrive at the present invention for a TFT device.

The same is true of the combination of the disclosures by Huang et al. and Kuo et al. That is, neither of the disclosures by Huang et al. or Kuo et al. contain any suggestion or provide any motivation to one of ordinary skill in the art to combine a DRAM cell device with an enhanced hot carrier effect MOSFET to obtain a TFT device having a polysilicon layer overlaid by a gate dielectric layer with improved parametric performance.

In view of the above discussion, Applicants respectfully submit that claims 1-19 should be allowable over the cited prior art references of Huang et al., Doklan et al. and Kuo et al., either alone or in combination, and that the rejection of claims 1-19 under 35 U.S.C. §103(a) is thus overcome. Applicants accordingly request reconsideration of claims 1-19 and that the obviousness rejection be withdrawn.

Applicants further note, as discussed above, that the disclosure by Yamazaki is not applied in the rejection of claims 1-19. In addition, Applicants note that it would not have been obvious to combine the teachings of Yamazaki with any of the other cited prior art references, especially since Yamazaki fails to disclose a polysilicon layer overlaid with a gate dielectric layer according to the present invention, as discussed in detail in the prior Office Action Response.

Conclusion

The Examiner in the most recent Office Action has applied all of the previous art in the same manner as the previous Office Action, and provides the additional disclosure of Kuo et al. to support the premise that claims 1-19 are unpatentable in combination with the other previously cited disclosures. However, the disclosure by Kuo et al. does not provide any new teaching with regard to the use of a polysilicon layer overlaid by a gate dielectric layer in forming a TFT device. Accordingly, Applicants submit that the present invention recited in claims 1-19 should be allowable over all the cited prior art references exclusive of the disclosure by Kuo et al., as provided in the response to the previous Office Action, and that the additional citation of Kuo et al., far from making the present invention unpatentable, serves to add cumulative information

and promote piecemeal prosecution of the present application. In addition, there is no suggestion in the references themselves for their combination, undermining any support suggested for a *prima facie* case of obviousness. MPEP 2142. Because Applicants respectfully believe that the present issues involved in the application could have been readily resolved prior to the previous Office Action, an interview with the Examiner is respectfully requested at the earliest convenient date and time with Applicants' undersigned representative.

It is respectfully believed that all issues in the most recent Office Action are addressed in this response, and that the application stands ready for allowance in view of the above discussion with regard to the cited prior art references. Early and favorable action on this application is respectfully requested.

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Kourosh Salehi
Name of applicant, assignee or Registered Representative

Kourosh Salehi
Signature

September 22, 2003
Date of Signature

KS/BJK:gl

Respectfully submitted,

Kourosh Salehi

Kourosh Salehi
Registration No.: 43,898
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700